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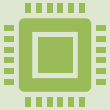
# IC Design Research & Development in Institut Teknologi Bandung

**Prof. Trio Adiono, PhD**

**University Center of Excellence on Microelectronics**
**Institut Teknologi Bandung**

Taiwan, 2 November, 2023

# Competency in IC Design



## Full Custom Design (Analog & Mixed Signal)

- Schematic Design
- Design Simulation
- Floorplaning and Placement and Routing

## Semi Custom

- Hardware Design Modeling
- Architecture Design
- RTL Design & Simulation

## System On Chip

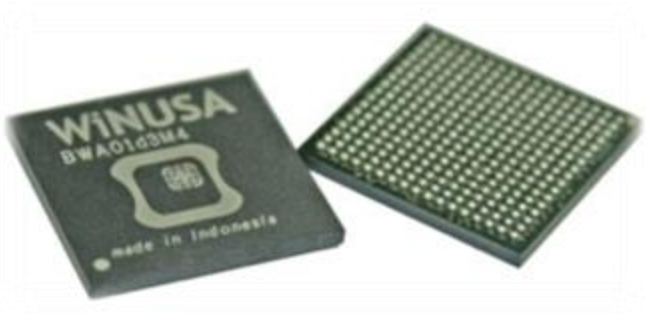
- Hardware & Software Co Design
- IP Design
- Integration of in-house IP, third party IP and foundry IP in SoC development

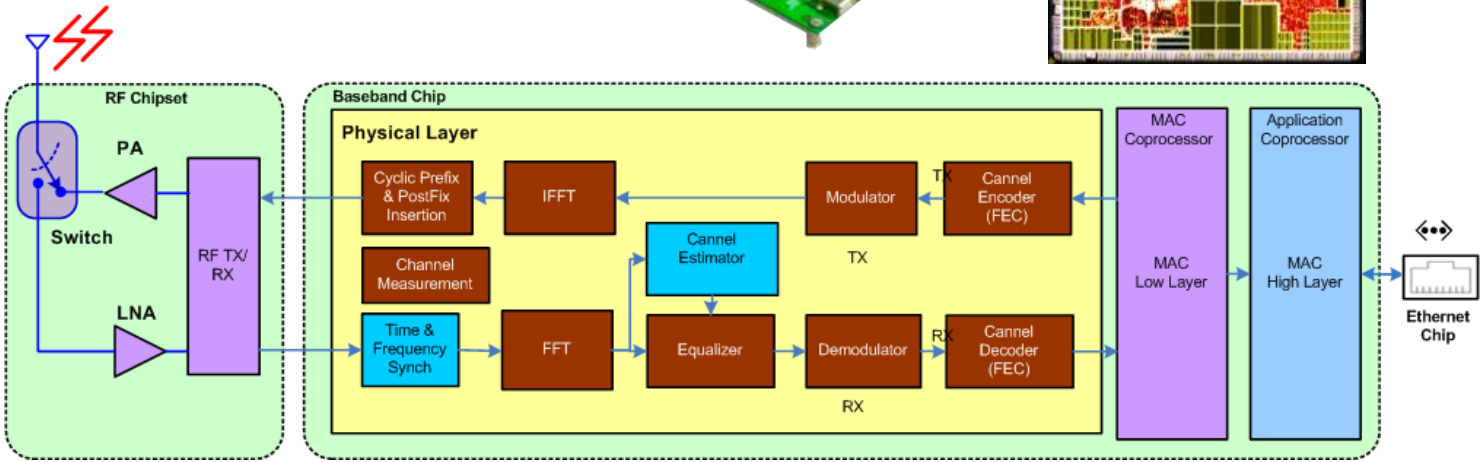
# Competency in Chip Design

- ASIC Front-End Design & Verification
  - Design Synthesis
  - Simulation (Functional, Gate and Full Timing)
  - Static Timing Analysis
- ASIC Back-End Design & Verification
  - Formal Verification
  - Static Timing Analysis
  - Floorplanning
  - Physical P&R
  - DRC/LVS
  - Parasitic Extraction
  - Crosstalk/IR Drop
- Design-For-Test
  - Memory, Functional BIST
  - SCAN Insertion/ ATPG
  - JTAG
- System Verification Planning
  - Verilog/SystemC
  - Directed Test and Assertion Based
- FPGA Prototyping
  - Design Synthesis and Optimization
  - In Circuit Verification

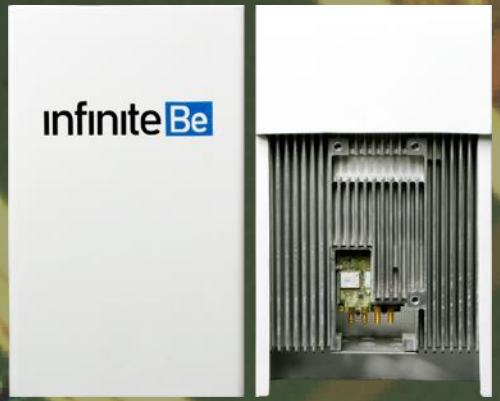
# RESEARCH & DEVELOPMENT

# Chip : Baseband Processor



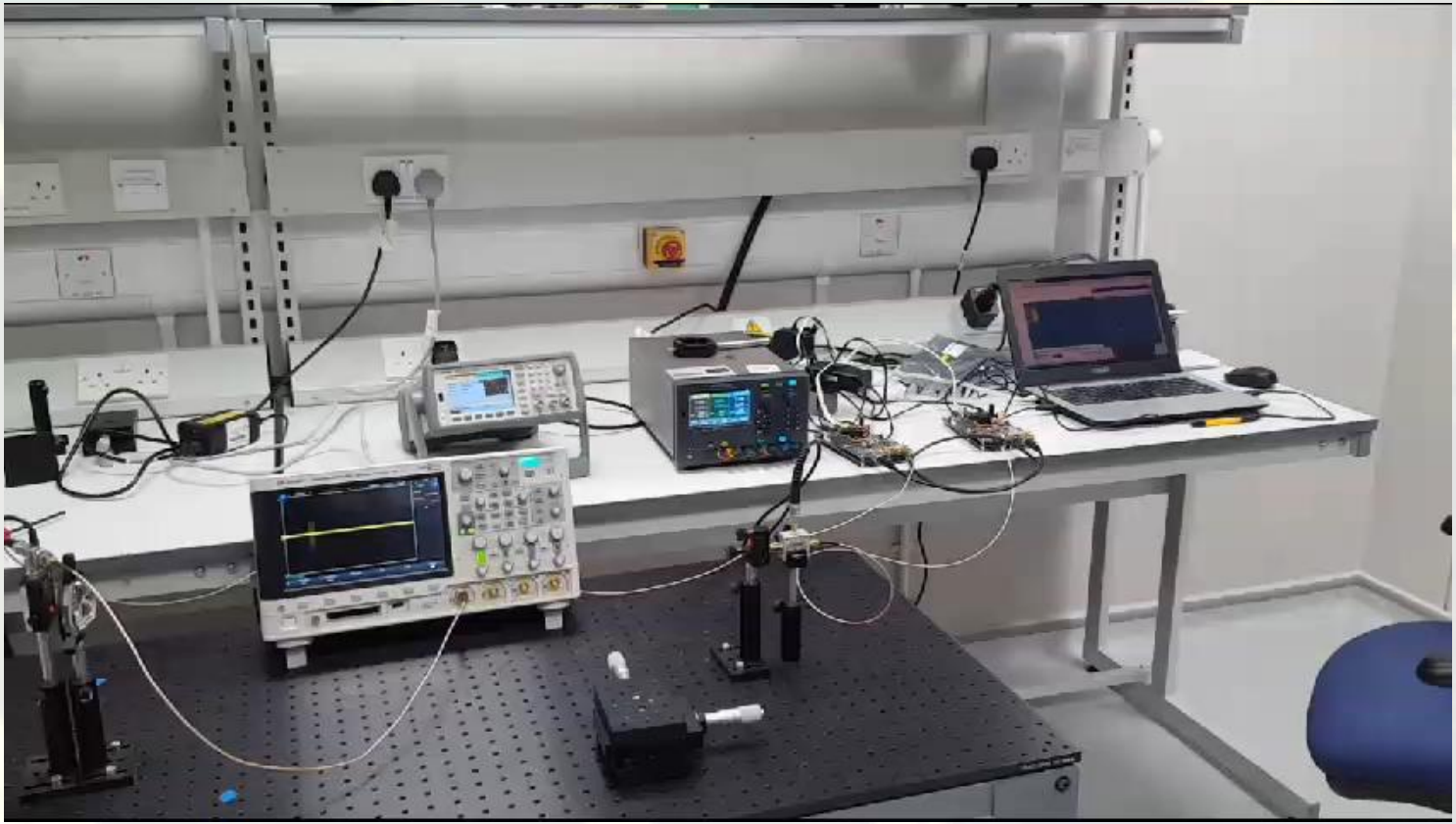
# Measurements/Prototyping



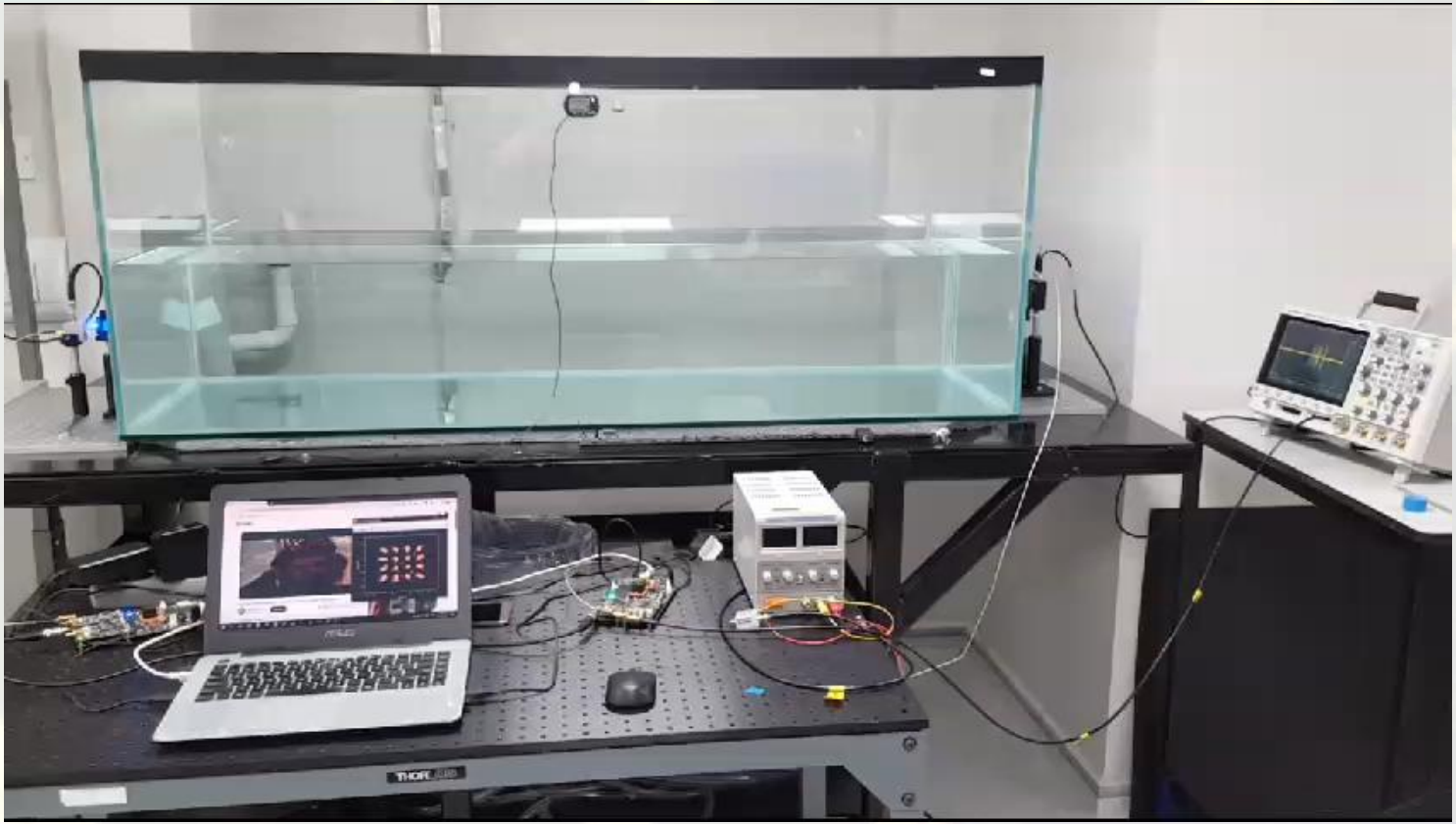

# Real-time Prototype

# Mashed Network Wireless Communications

# Real-Time Performance Measurement (RED LED)

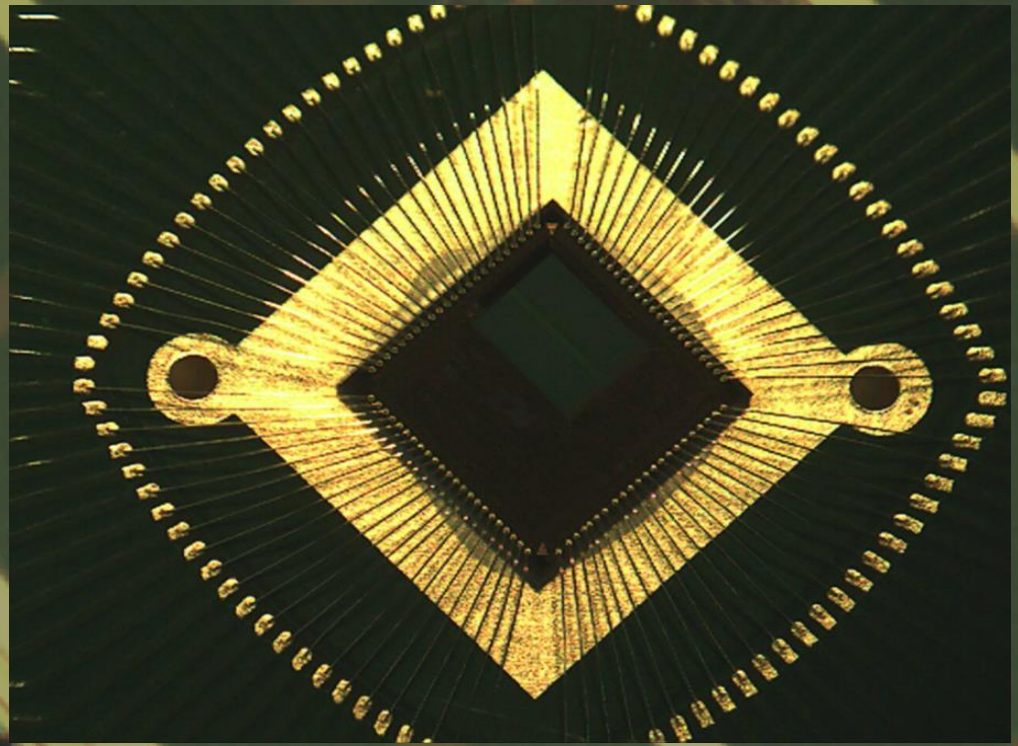


# Real-Time Under Water Communication

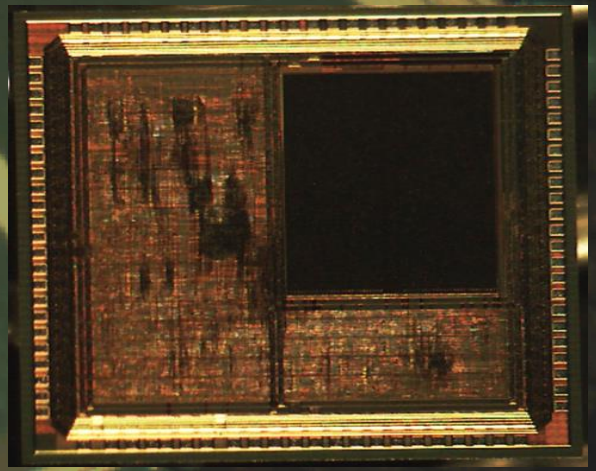


# NEAR FIELD COMMUNICATION

# NFC Chip Silicon Dies

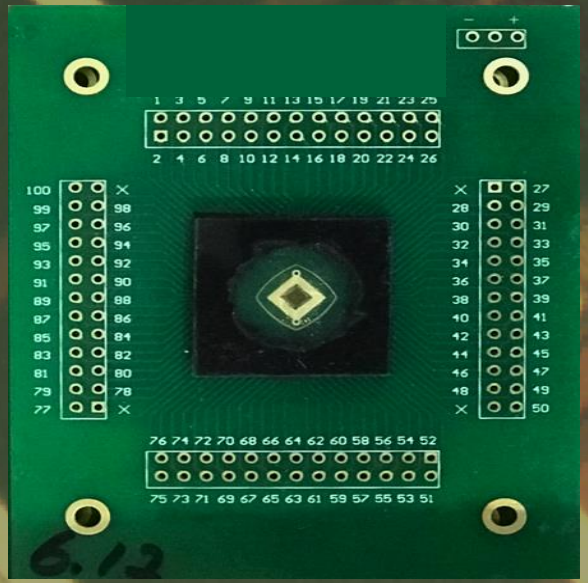


Chip Bonding

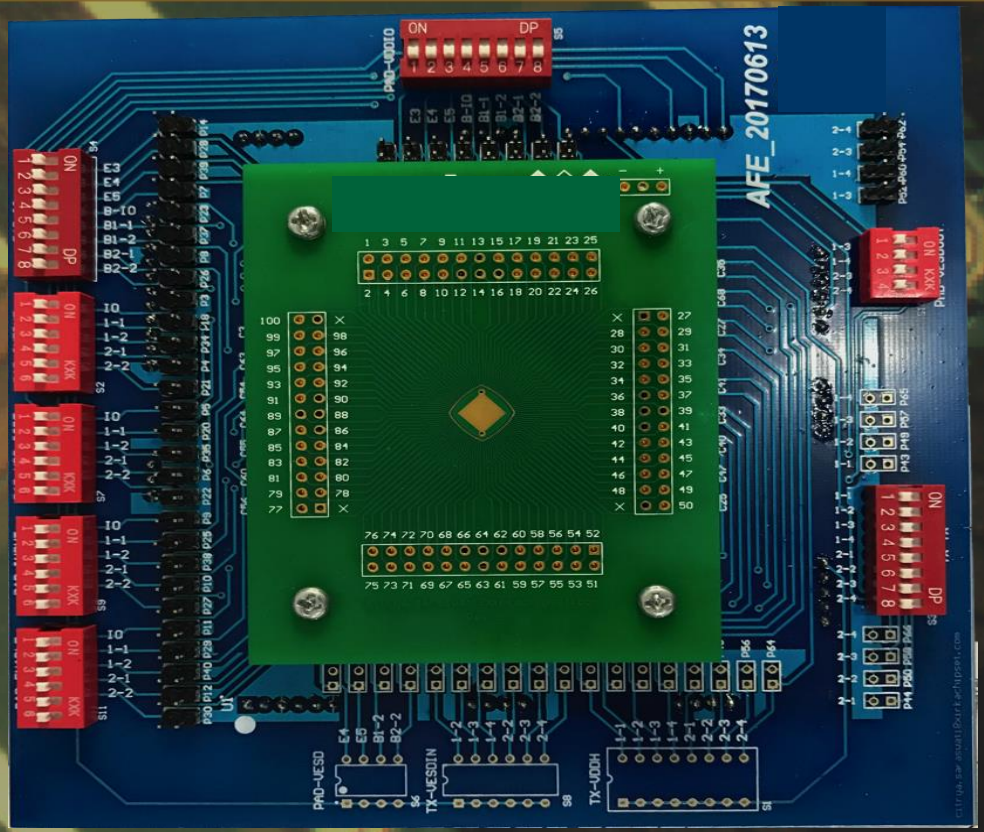


Silicon Die

# Chip Testboard & CoB



Chip On Board (COB)



# NFC Communication

# Analog Design Layout PLL

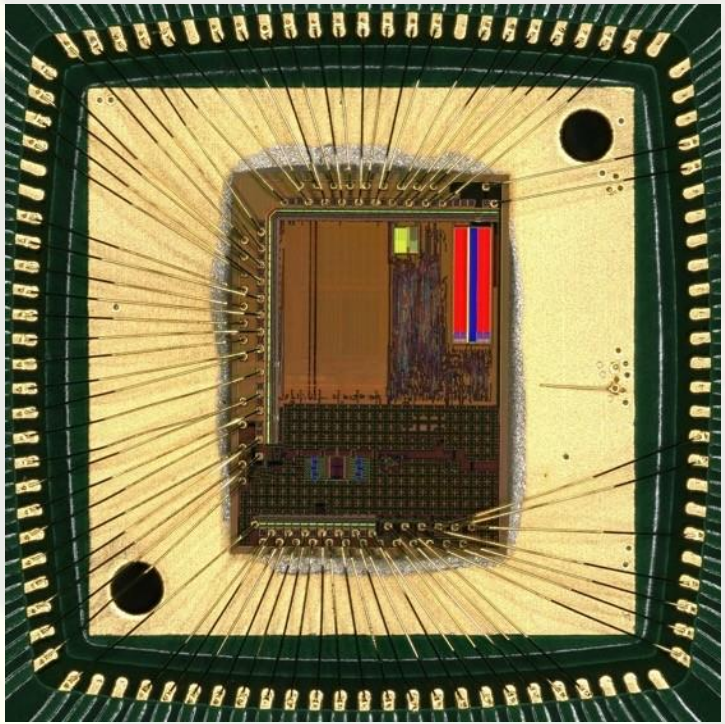
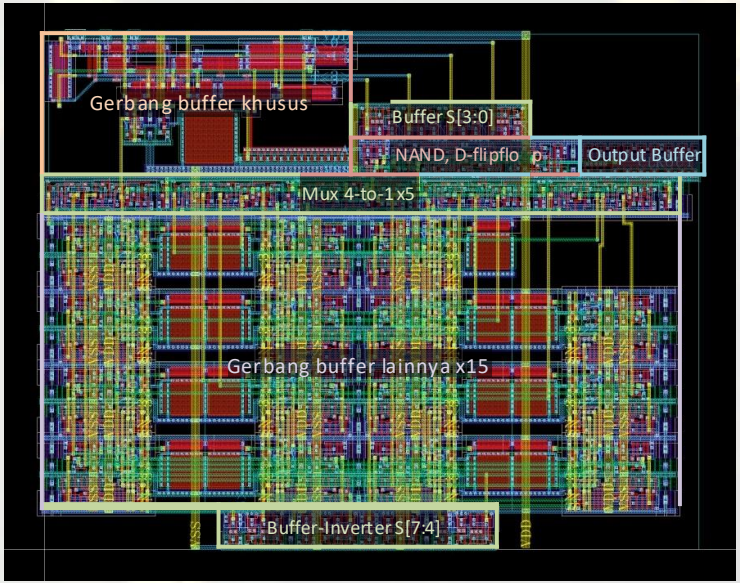


Foto mikroskopik dari *chip* osilator terkendali yang dimuat di atas *Circuit-on-Board*.



# Artificial Intelligence Research

## Supervised Learning

### Low Latency YOLOv3-Tiny Accelerator for Low-Cost FPGA Using General Matrix Multiplication Principle

TRIO ADIONO[1,2], (Member, IEEE), ADIWENA PUTRA[2], NANA SUTISNA[1,2], (Member, IEEE), INFALL SYAFALNI[1,2], (Member, IEEE), AND RAHMAT MULYAWAN[1,2], (Member, IEEE)
[1]Electrical Engineering Department, School of Electrical Engineering and Informatics, Institut Teknologi Bandung, Bandung, West Java 40116, Indonesia
[2]University Center of Excellence on Microelectronics, Institut Teknologi Bandung, Bandung, West Java 40132, Indonesia



### Fast and Scalable Multicore YOLOv3-Tiny Accelerator Using Input Stationary Systolic Architecture

Trio Adiono, *Senior Member, IEEE*, Rhesa Muhammad Ramadhan, *Student Member, IEEE*, Nana Sutisna, *Member, IEEE*, Infall Syafalni, *Member, IEEE*, Rahmat Mulyawan, *Member, IEEE*, and Chang-Hong Lin, *Member, IEEE*

## Unsupervised Learning

### FARANE-Q: Fast Parallel and Pipeline Q-Learning Accelerator for Configurable Reinforcement Learning SoC

NANA SUTISNA[1,2], (Member, IEEE), ANDI M. RIYADHUS ILMY[1], INFALL SYAFALNI[1,2], (Member, IEEE), RAHMAT MULYAWAN[1,2], (Member, IEEE), AND TRIO ADIONO[1,2], (Senior Member, IEEE)
[1]School of Electrical Engineering and Informatics, Institut Teknologi Bandung, Bandung, West Java 40132, Indonesia
[2]University Center of Excellence on Microelectronics, Institut Teknologi Bandung, Bandung, West Java 40132, Indonesia

## Security

### Efficient Homomorphic Encryption Accelerator With Integrated PRNG Using Low-Cost FPGA

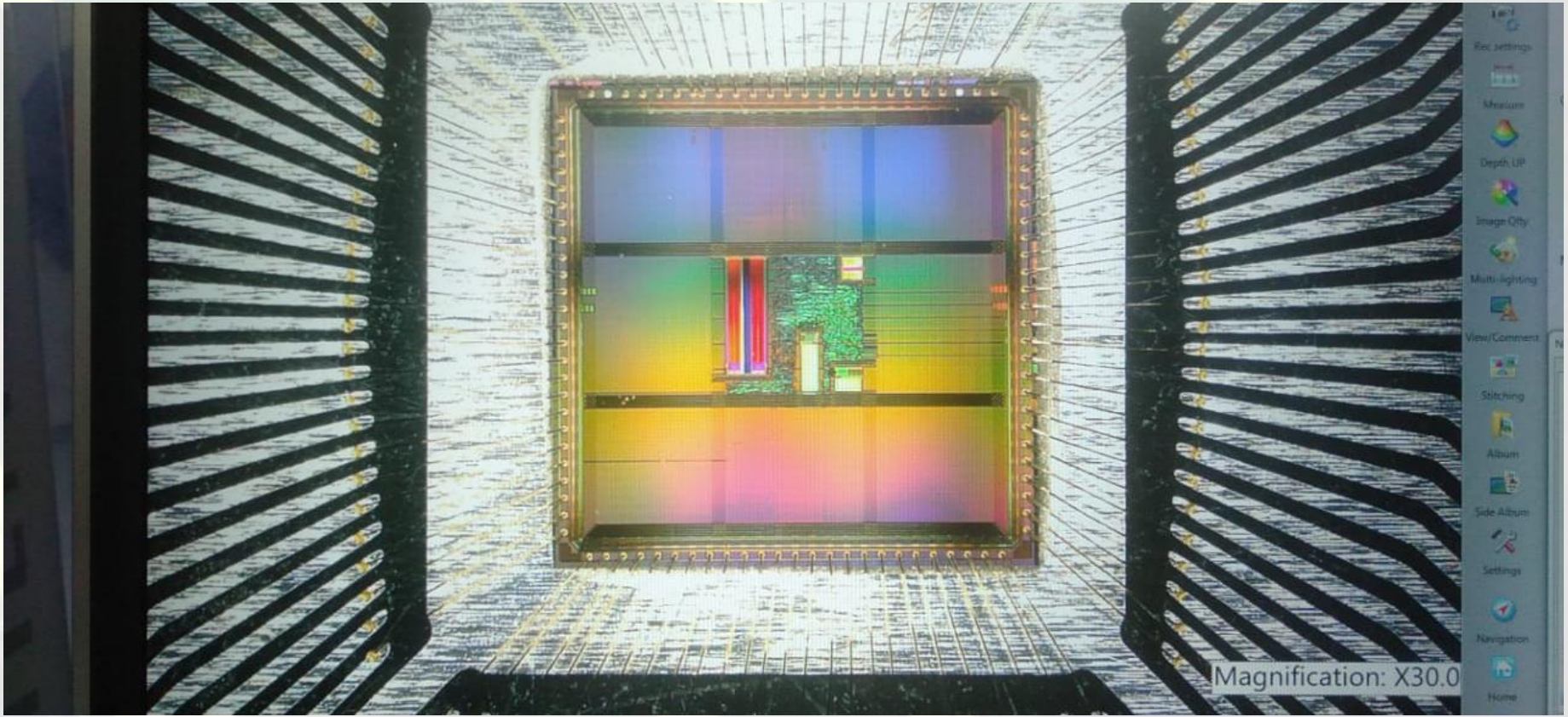
Publisher: IEEE Cite This PDF

Infall Syafalni ; Gilbert Jonatan ; Nana Sutisna ; Rahmat Mulyawan … All Authors


# Artificial Intelligence Chip

**Lab IC Desain**
**Pusat Mikroelektronika ITB**

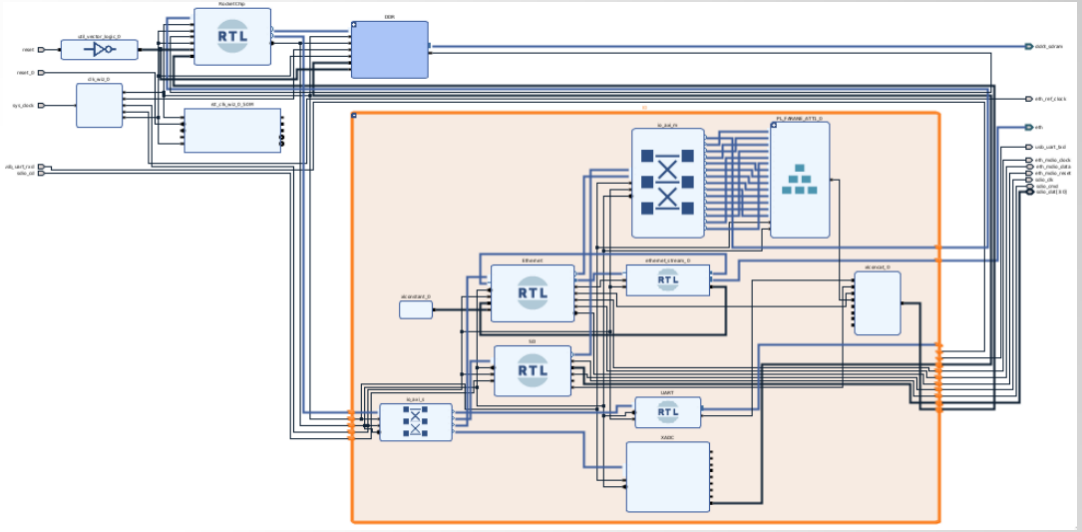
# IoT Chip Die

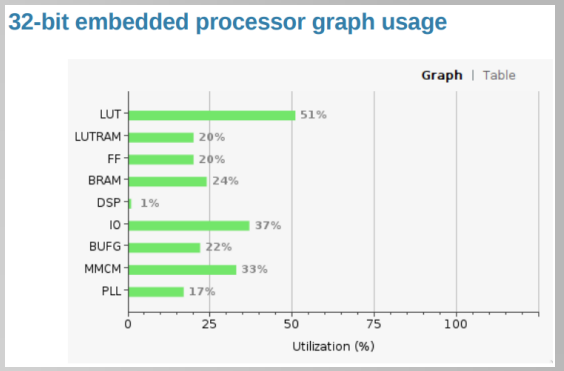


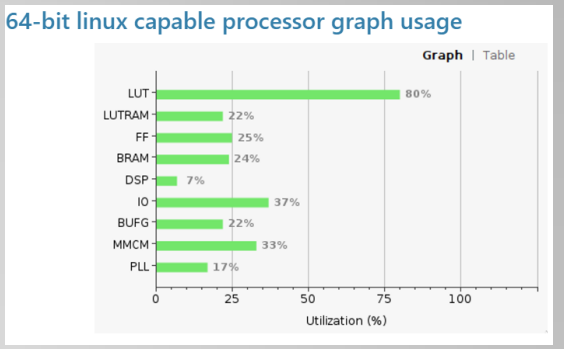
# Modul Sensor

# RISCV+AI Accelerator

Hardware: RISC-V Softcore to FARANE-Q Implementation

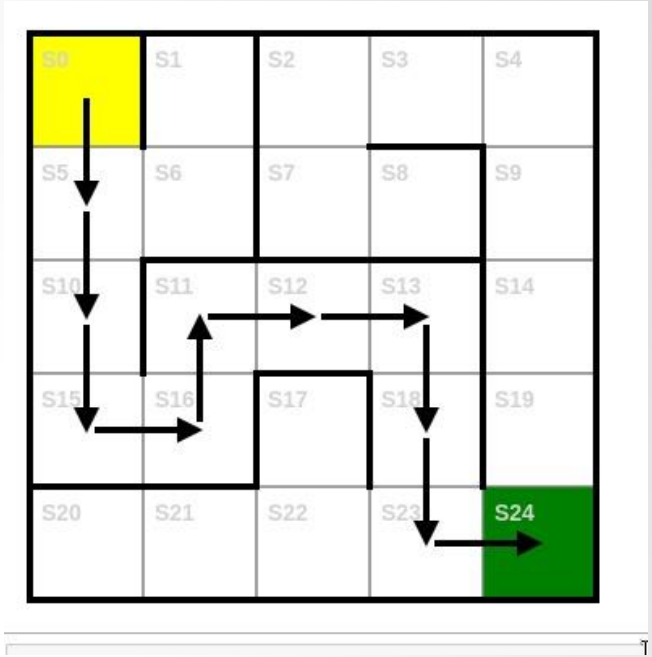


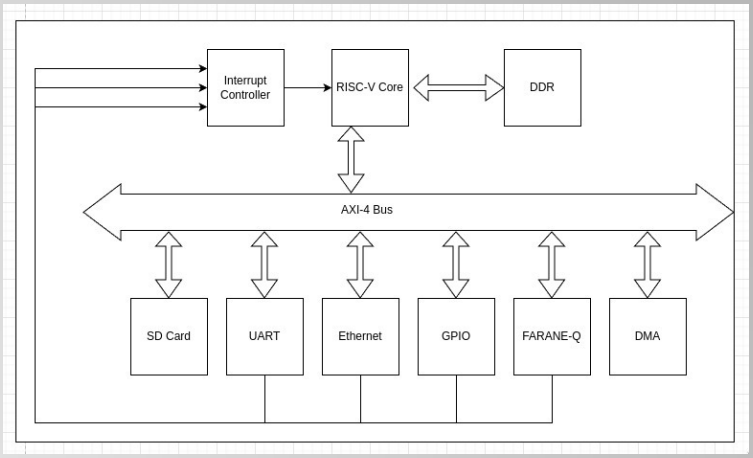



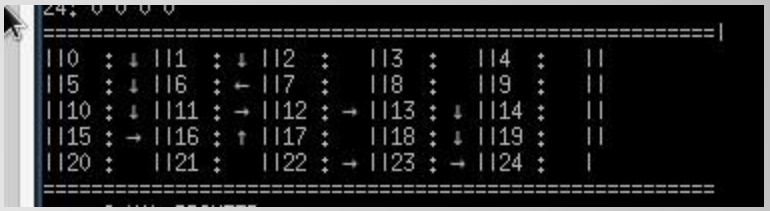



# Reinforcement Learning

Software: PYNQ's Jupyter-notebook to C conversion



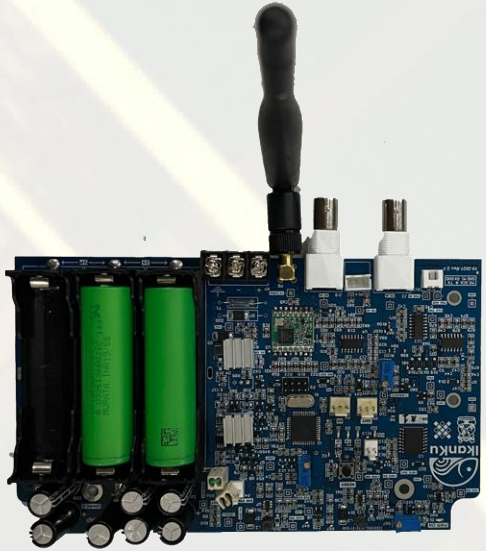
# INDUSTRIAL COLLABORATION

# Energy Meter


## Smart Energy Meter


## DLMS Energy Meter Modem

# Internet Of Things (IoT)




**Water Quality**

# Medical : Smart Pump

## Syringe Pump

## Infusion Pump

# Medical : Cardio



**Patient Monitor**

# Medical : Spirometer


Direct contact with patients using temperature sensors, SPO2, and respiratory sensors (mouthpiece).


Android & IOS App

Control patient device functionality, record data to the cloud and real-time monitor measurement results.


# Awards

- LSI Design Contest, 2014, Japan, 1st Winner,
  *"Smart Info Media (SIS) Award"*.
- 1st Award (SIS Award), 2009 LSI Design Contest, Okinawa
- 3th Award (Xilinx Award), 2009 LSI Design Contest, Okinawa
- Asia Pacific Information Technology Award (APICTA) 2008
- IEICE, Communication Society Award, 2008 LSI Design Contest, Okinawa
- Semiconductor Industry News Paper Award, 2008 LSI Design Contest, Okinawa
- The Best Feature Award, 2007 LSI Design Contest, Okinawa
- The Best Feature Award, 2006 LSI Design Contest, Okinawa







# Innovation Park Bandung Teknopolis


| Building Name | Number of Floors | Building Area (m2) |
|---|---|---|
| 1st Building | 13 | 18.099 |
| 2nd Building | 12 | 12.038 |
| 3rd Building | 11 | 8.815 |
| 4th Building | 11 | 2.720 |
| TOTAL | | 44.551 |

**Smart Industry Creative Center**
**Focus on Industry 4.0**

Artificial Intelligence, *Internet of Things, Virtual Reality, 5G, and Big Data*

**Urgency of Development:**

1. Provision and management of clean laboratories for Industry 4.0 innovation products
2. Facilities for innovation research activities to produce industrial scale products

| Building | Building Area (m2) | Status |
|---|---|---|
| 1st & 2nd Building | 6.027 | Has been granted and received land certificate |
| 3rd & 4th Building | 3.873 | Land grants in 2023 according to the progress of the 1st & 2nd |

**As part of Major Project National Perpres No.18/2020, start of construction in 2021-**

Center
.itb.ac.id
ry partners

# Innovation Park Bandung Teknopolis | Mapping Plan for Equipment Support and Industrial Innovation Research

## Building 2

Equipment Procurement Cost : USD 2.788.580

**11th Floor (930m2)**
Computed Tomography

**7th Floor (675m2)**
Defense & Security Technology

**4th Floor (675m2)**
Coding School

**10th Floor (1130 m2)**
EMC Testing, Battery Testing & Electric Componpents Bench Testing

**6 & 5 th (1350m2)**
Incubator & Accelerator

**Ground Floor (150m2)**
Dynotest Facilities

## Masterplan Design


## Building 1

Equipment Procurement Cost : USD 4.748.122

**11th Floor (1.465 m2)**
Stem Cell & Eksosom Lab

**10th Floor (1.465 m2)**
Transportation & Vehicle Lab

**8th Floor (1.456 m2)**
Bioinformatics Lab

**6th Floor (1.456 m2)**
PCB Tech & IC Design Center

**3 & 4th Floor (2.8108 m2)**
Catalyst & Anchor Industry Research Center & Commercial Area

**12-13th Floor (2.565 m2)**
Radar & Technopark Dormitory

**9th Floor (1.465 m2)**
Smart City & Command Center

**7th Floor (1.456 m2)**
AI Design Center & Tectonic Modelling

**5 & 4th Floor (2.856 m2)**
Mini Wafer Fabrication

**GF & Public Outdoor Space (300 m2)**
Charging Station

## Building 3

**9-10 Floor (1980m2)**
Cyber Physical System Lab

**8th Floor (990 m2)**
Digital Security & Forensics

**7 & 6th Floor (1930 m2)**
Open Innovation Lab.

**4 & 5 Floor (1700 m2)**
Anchor Industry.

**GF, 1 & 2 Floor (1700 m2)**
Function Hall & Commercial Area

## Building 4

**10 & 11th Floor (900m2)**
Co-Working Spaces

**9th Floor (600 m2)**
Additive Manufacturing Lab

**4 & 5th Floor (1100 m2)**
Incubator & Accelerator

**2 & 3rd Floor (1100 m2)**
Commercial Area, Café & Lounge

# International University Networks

- Tokyo Institute of Technology, Japan
- Shibaura Institute of Technology, Japan
- Keio University, Japan
- University of Twente, Netherlands, SPIN Mobility Program
- NNTTF (National Networked Tele Test Facility for Integrated System)-Australia
- University Sains Malaysia, Malaysia
- Kyushu Institute of Technology, Japan
- Kumoh National Institute of Technology, Korea
- Japan Advance Institute of Technology, JAIST
- Pukyong Nationbal University, Korea
- Eidenburg, UK
- National Taiwan University of Science and Technology
- Korea Advance Institute of Science and Technology